WHAT IS CLAIMED IS:

1. A multiprocessor apparatus comprising:

a high speed processor operating at a high speed;

a low speed processor operating at a low speed; and

an activation controller for controlling activation and inactivation of each of said high speed processor and said low speed processor based on application program to be processed.

2. The multiprocessor apparatus according to claim 1, further comprising a processing determining unit for determining as to at which of said processors application program is to be processed, wherein said activation controller controls activation and inactivation of each of said high speed processor and said low speed processor based on a determination result of said processing determining unit.

3. The multiprocessor apparatus according to claim 1, further comprising a bus coupling unit which couples a high speed bus for coupling said high speed processor and a low speed bus for coupling said low speed processor, wherein said bus coupling unit includes a switch coupled to a memory, for switching connection and disconnection between said memory and said high speed bus.

4. The multiprocessor apparatus according to claim 1, further comprising: a memory coupled to said high speed bus for storing data and program required for said high speed processor to process said application program; and a memory coupled to said low speed bus for storing data and program required for said low

speed processor to process said application program.

5. The multiprocessor apparatus according to claim 4, further comprising a memory which stores data and program necessary for transferring said data and program required for said low speed processor to process said application program from said memory coupled to said high speed bus to said memory coupled to said low speed bus.

6. The multiprocessor apparatus according to claim 4, further comprising a DMA circuit for transferring said data and program required for said low speed processor to process said application program from said memory coupled to said high speed bus to said memory coupled to said low speed bus.

7. The multiprocessor apparatus according to claim 4, wherein said low speed processor transfers said data and program required for said low speed processor to process said application program from said memory coupled to said high speed bus.

8. The multiprocessor apparatus according to claim 1, wherein said activation controller includes a clock switch for activating and stopping clock signals for said respective processors.

9. The multiprocessor apparatus according to claim 1, wherein said activation controller includes a poser source switching for activating and stopping power sources for said respective processors.

10. The multiprocessor apparatus according to claim 1,

wherein said low speed processor has minimum function required for processing said application program at a low speed.

11. The multiprocessor apparatus according to claim 1, wherein said low speed processor is set in a manner that operation voltage thereof is set to a low value and a frequency of a clock signal supplied thereto is set to a small value.

12. The multiprocessor apparatus according to claim 3, wherein said bus coupling unit includes a register, and said bus coupling unit changes contents of said register based on a result of determination of said processing determining unit, and said activation controller controls an activation state of said processor based on contents of said register.

13. The multiprocessor apparatus according to claim 1, wherein said low speed processor requires said activation controller to make said low speed processor inactivate after completion of processing of said application program.